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The chemistry of the compound semiconductor – intrinsic insulator interface

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Abstract. Processes leading to the growth of intrinsic insulators (oxides, sulfides, and fluorides) on the surfaces of semiconductors of the III–V, II–VI, and IV–VI groups as well as their solid solutions are analysed with the aid of classical thermodynamics. Their phase compositions, found from the equilibrium phase diagram, are compared with the compositions found as a result of experimental studies of the semiconductor–insulator interface. It is shown that there is a relation between the characteristic features of the equilibrium phase diagram (in particular the segregation of a metal or nonmetal at the interface), the type of intrinsic lattice defects, and the electrophysical properties of the interface. The possible ways of creating an ideal compound semiconductor–insulator interface are considered. The bibliography includes 171 references.

I. Introduction

Oxidation is one of the first chemical reactions which humanity encountered at the dawn of history. With time, the number of known metals increased and the requirements which they had to meet became more stringent, but the problem remained in essence the same: how to protect finished articles from the destructive effect of the environment. Two main approaches were used. The first reduced to the search for a metal which would not be oxidised at all and it is not fortuitous that such metals have been called noble. The second involved the transformation of the enemy into a friend, i.e. the finding of an oxide which would serve as a protection. Aluminium oxide may serve as a successful example.

When it was proposed that the surface of silicon semiconductor devices be protected by silicon dioxide SiO_2, nothing new took place. However, when the first transistor based on a metal–oxide–semiconductor (MOS) system was created, the layer of oxide became an active component of the device itself and fundamentally new requirements, concerning primarily electrical parameters, were formulated for it. Almost all the electrical properties of the semiconductor–oxide interface are determined not by the bulk-phase characteristics of the oxides but by the extremely thin transition region, with a thickness of several nanometers, between the oxide and silicon, which contains a boundary phase with unusual composition and coordination of the silicon and oxygen atoms. Chemical engineering was therefore faced with the problem of regulating, with hitherto unheard of accuracy, the composition and structure of the interface formed on the surface of the conductor during oxidation.[1]

The problem of optimising the properties of the $Si–SiO_2$ interface was solved successfully and for the best MOS transistors the concentration of the electrically active defects on the interface does not nowadays exceed one defect per $10^4–10^6$ surface silicon atoms.† Nowadays the structure and properties of the $Si–SiO_2$ interface have been investigated in great detail, which is best indicated by the advances in silicon electronics. The relative simplicity of the technology, compactness, and the low power required by circuits based on MOS transistors made them irreplaceable in the manufacture of microprocessors and memory circuits, the wide scale employment of which determines in many respects the current progress in science and engineering.

The advance achieved in the development of silicon electronics permits one to hope that it will be repeated in the creation of devices based on binary semiconductors, particularly bearing in mind that the problems of regulating the bulk-phase properties have already been solved for most of them. This applies primarily to GaAs, in which the electron mobility is six times higher, its radiation stability is greater, and its working temperature range is wider (from −200 to 200 °C) compared with silicon. All this leads to most extensive prospects for the creation of ultrafast integrated circuits. The reason why these prospects have not been fully realised hitherto is mainly associated with the failure of the attempts, over a period of almost 30 years, to create a gallium arsenide–insulator interface the parameters of which would be close to those of the $Si–SiO_2$ interface.‡ In many respects this is

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† We may note that a method for the modulation of the electrical conductivity in the surface layer of the material, which constitutes the basis of the operation of MOS transistors, was patented as early as 1926, but, owing to the lack of ability to regulate the properties of the surface, it could not be applied in practice for a long time.

‡ At the Jubilee XXth Conference on the Physics and Chemistry of Interfaces in Semiconductors (USA, 1992), it was noted that the reason for the failures is the complexity of the chemistry of the GaAs surface.[2]

associated with the much more complex chemical composition of the boundary phases. Thus the chemistry of interfaces has become a crucial problem in the creation of microelectronic devices based on compound semiconductors.

Valuable results of this kind have been obtained for III–V semiconductors using the methods of classical thermodynamics. With the aid of these methods, it has been possible to predict at the microlevel the phase composition of the interfaces, which is, generally speaking, unexpected for a macroapproach of this kind. There has been recently a certain renaissance of thermodynamic methods. Nowadays, when it is possible to determine experimentally with the aid of electronic and ionic spectroscopy the composition and structure of interfaces at the atomic level, it has been found that thermodynamic calculations make it possible to analyse extremely effectively such complex systems. Thus thermodynamic calculations have in fact successfully predicted the sequence in the formation of phases on interaction in metal–silicon structures.[3] Thermodynamic analysis of the oxidation of the test material in order to determine the phase composition of the intrinsic oxide on the semiconductor–oxide interface is of interest for MOS structures. One of the simplest procedures used successfully in such analysis involves the calculation of phase equilibrium diagrams for the semiconductor–oxygen system. This approach was in fact first used to analyse the oxidation of the surfaces of semiconductors of the III–V group by Schwartz[4] and members of the Institute of Inorganic Chemistry of the Siberian Division of the USSR Academy of Sciences[5] at the beginning of the 1980s; later it was extended to other semiconducting compounds.

It must be emphasised that at the present time the range of insulators which are potentially suitable for the creation of devices based on metal–insulator–semiconductor (MIS) systems has greatly expanded. These are not only oxides but also other intrinsic insulators, i.e. compounds during the formation of which the semiconductor atoms are incorporated in the composition of the growing layer of the insulator.[6] The interface between the semiconductor and such compounds has also been analysed successfully with the aid of the phase equilibrium diagram.

This review is devoted primarily to the analysis of the application of phase equilibrium diagrams in the description of the interaction of oxygen with binary semiconductors and solid solutions based on them. Attention is concentrated on the establishment of a relation between the chemistry of the interface and its electrophysical parameters since only the understanding of this relation will make it possible to create promising devices based on compound semiconductors.

II. Thermodynamic analysis of the compound semiconductor – intrinsic insulator interface

There is a definite relation between the advances in the silicon MOS technology and the relative simplicity of the chemical processes occurring in the oxidation of silicon.[1,7–9] Indeed, in terms of their chemical composition and structure, the SiO_2 layers on silicon resemble vitreous silicon dioxide (fused quartz), are characterised by a high degree of chemical uniformity, and correspond to the stoichiometric formula SiO_2 almost throughout the thickness of the layer. Only at the interface between the Si and SiO_2 phases, which have different crystal structures and chemical compositions, the surface regions of both materials are reconstructed, some of the surface chemical bonds are rehybridised, and new chemical groups (characteristic of the interface alone), in which silicon has the Si^{3+}, Si^{2+}, and Si^{+} oxidation states, are formed. The thickness of the transitional region, having the composition SiO_x ($x < 2$), does not exceed several nanometers. Although the SiO_2 layer, having a thickness of 1.5–3.0 nm, adjoining this transitional region does have the stoichiometric composition, it is nevertheless mechanically strained owing to the nonidentity of the lattice constants of silicon and SiO_2. The structure of two monolayers of silicon atoms adjoining the interface is disturbed on the side of the silicon support. It is assumed that the defects in the transitional SiO_x region actually determine many of the electrical parameters of the interface.§ Bearing in mind the deficiency of oxygen in the transition layer, one can assume that such intrinsic defects may be oxygen vacancies and the ruptured bonds involving silicon atoms (the so called trivalent silicon).

Overall, the picture of the $Si–SiO_2$ interface proved to be fairly complex and it was necessary to develop unique experimental methods in order to be able to characterise it fully.

Proceeding to the consideration of the chemistry of interfaces involving compound semiconductors, it must be emphasised that the problem of the formation of the $Si–SiO_2$ interface actually reduces merely to the correspondence between the crystal lattices of two single-phase stoichiometric materials, the problem being facilitated by the fact that one of them possesses fairly flexible interatomic bonds, the angle between which can vary within wide limits.

In the case of a binary semiconductor, the problem is immeasurably more complex: two elements are now oxidised, each of which can have several oxides and some of the oxides can be variable-composition phases. Furthermore, if the oxide of one of the elements is highly basic whilst that of the other is highly acidic, a salt is formed and the number of complex oxide phases, for example phosphates, can also be large. All this leads to a multiphase structure of the oxide layer, which is usually accompanied also by a spatial nonuniformity. Furthermore, under certain conditions, chemical interaction of the oxide phases not only with one another but also with the semiconductor support becomes possible. As will be shown below, by employing phase equilibrium diagrams, it is possible to predict the composition of the oxide layer and, what is especially important, of the compound semiconductor–intrinsic insulator interfaces.

The method of phase equilibrium diagrams is based on the analysis of the possible interactions in the test materials–oxygen system. For a two-component compound AB, the interaction of the phases in the A–B–O ternary system, represented by the Gibbs triangle, is considered. The specific form of the phase equilibrium diagrams for the III–V, II–VI, and IV–VI compounds considered in this review is presented in Fig. 1.

All the oxide phases in the A–B–O system are assumed to be pure individual compounds and only condensed phases under standard conditions are considered. The miscibility of the phases is neglected. The chemical reactions occurring between pure phases are therefore studied, so that the phase equilibrium diagram for the A–B–O system contains only straight lines connecting the phases pairwise. These lines represent the thermodynamic equilibrium states between the phases. The stability of the lines is estimated from the Gibbs free energies of the chemical reactions (ΔG) recorded at the point of intersection of the lines, the line connecting the products of the reactions with $\Delta G < 0$ being regarded as stable. The calculation of ΔG requires a knowledge of the standard molar Gibbs free energies of formation ΔG° of all the phases belonging to the A–B–O system. Since the free energies ΔG° are by no means known for all substances, a series of methods have been developed for the estimation of these quantities (see, for example, Barin et al.[14]).

The phase equilibrium diagram can be used, firstly, for the estimation of the phase composition of the oxide film formed on the surface of the test compound during reversible oxidation in dry oxygen. The number of phases and their spatial distribution in the bulk of the oxide film can be found by analysing the line connecting oxygen and the test material and by analysing the question of which phase regions are intersected by this line.

§ The properties of the interface, like those of the insulator itself, can be regulated with the aid of impurity atoms. A review has been devoted to this problem.[10]

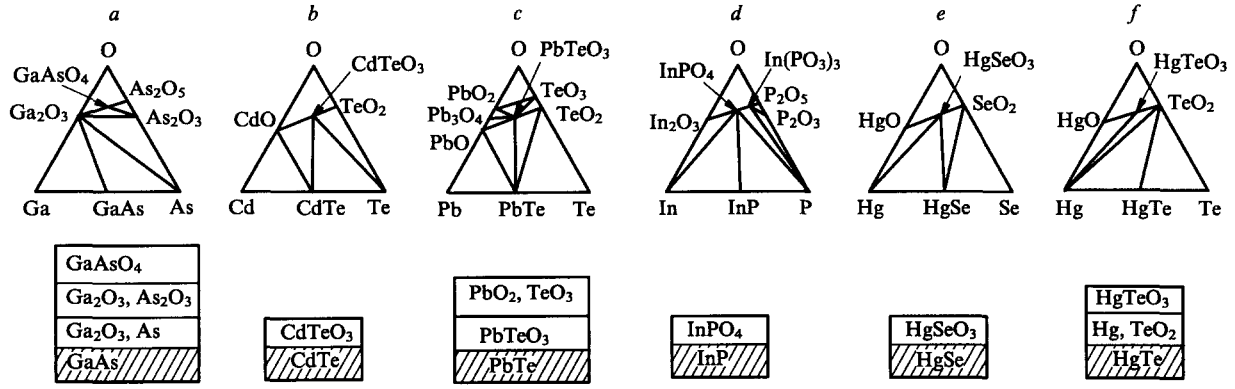


Figure 1. Phase equilibrium diagrams and phase composition profiles for the intrinsic oxides in various systems: (*a*) Ga–As–O;[4] (*b*) Cd–Te–O;[11] (*c*) Pb–Te–O;[12] (*d*) In–P–O;[4] (*e*) Hg–Se–O;[13] (*f*) Hg–Te–O.[11]

The chemical potential of oxygen is lowest at the semiconductor–oxide interface, increases monotonically along the thickness of the oxide film, and reaches a constant value in the gas phase. Consequently, movement along the line from the test compound, located at the base of the phase equilibrium triangle, to the apex of the diagram describes in succession the phase composition of the semiconductor–oxide interface and of the bulk-phase and surface components of the oxide film.

Another important practical application of phase equilibrium diagrams involves the possibility of predicting the chemical interaction of the oxide films formed with the support. It was noted above that the chemical potential of oxygen decreases monotonically from the oxide–gas phase interface to the support–oxide interface. The oxide film is formed until its thickness reaches a value for which the chemical potential of oxygen diminishes to a critical value which is insufficient for further growth of the oxide. If gaseous oxygen is removed (such a situation actually arises when the oxidised material is annealed *in vacuo* or under an inert gas atmosphere), then the oxide phases which are not linked by stable lines on the phase equilibrium diagram with the semiconductor may serve as the oxidant.

At the same time the method suffers from a fundamental limitation. The phase equilibrium diagram refers to a state of thermodynamic equilibrium and in no way describes the kinetics of the oxidation process. It provides a fundamental answer to the question of the possibility of the spontaneous occurrence of chemical reactions in the material–oxygen system investigated but does not indicate the time during which they take place. In practice, this means that the phase equilibrium diagram describes adequately the composition of the oxide film when the growth of the latter is sufficiently slow, so that its phase composition is determined by thermodynamic and not kinetic factors.

Additional complications in comparing data obtained by the method of phase equilibrium diagrams with experimental results may arise from the volatility of the oxide phases and their thermal decomposition or solubility, depending on the specific method used to oxidise the material.

A multiplicity of different versions of the structure of phase equilibrium diagrams is possible. For the binary semiconductors considered, six fundamentally different types of such diagrams are so far known. They are arranged in Fig. 1 in an order which reflects the transition from the preferential oxidation of the metal at the semiconductor–oxide interface in GaAs (Fig. 1*a*), through the synchronous oxidation of both components of the semiconductor with formation of a single complex oxide compound (Figs. 1*b*–1*e*), to the preferential oxidation of the nonmetal in HgTe (Fig. 1*f*).

We shall deal in greater detail with the diagram for GaAs bearing in mind that indium arsenide, indium and gallium antimonides,[4] as well as tin,[12] zinc,[13] and manganese[15] selenides and tellurides have qualitatively similar phase diagrams. When GaAs is oxidised, Ga_2O_3 and elemental arsenic are formed near the interface and the oxide consists of Ga_2O_3, As_2O_3, and $GaAsO_4$ (Fig. 1*a*). Thus, using the Ga–As–O phase equilibrium diagram it is possible to predict the formation of elemental arsenic at the GaAs–oxide interface as the phase corresponding to thermodynamic equilibrium. A similar conclusion concerning the preferential oxidation of the metal and the possible presence of the nonmetallic component in an elemental form at the semiconductor–oxide interface is also reached from the analysis of the analogous phase equilibrium diagrams for InAs, InSb, GaSb, SnTe, SnSe, ZnTe, ZnSe, MnTe, and MnSe. The phase equilibrium diagram for the Ga–As–O system also permits the technologically important conclusion that chemical reactions are possible between the semiconductor and the intrinsic oxide. Indeed, GaAs is linked on the phase equilibrium diagram by a stable line only with Ga_2O_3, i.e. the contacts between GaAs and arsenic oxides correspond to thermodynamic disequilibrium. If GaAs is linked by imaginary straight lines to As_2O_3, As_2O_5, or $GaAsO_4$, then the latter all intersect the stable Ga_2O_3–As line. This means that the oxidised arsenic is unstable in contact with GaAs and the chemical reactions occurring lead to the enrichment of the interface in elemental arsenic.

The phase equilibrium diagram for the Cd–Te–O system (Fig. 1*b*) has a fundamentally different structure. It contains the stable CdTe–$CdTeO_3$ line, which means that the oxidation of CdTe results in the formation of only one oxide compound — $CdTeO_3$. As for GaAs, the metal oxide is linked to the semiconductor by a stable line on the phase equilibrium diagram and the reaction between CdTe and TeO_2 can lead to the appearance of elemental tellurium in the region of the interface. Thus the CdTe–oxide interface is thermodynamically stable when the entire oxidised tellurium is in $CdTeO_3$.¶

PbTe undergoes yet another important change on the phase equilibrium diagram (Fig. 1*c*). Here the semiconductor is linked by stable lines to the first oxides of lead and tellurium and also to lead tellurite $PbTeO_3$. The PbTe–oxide interface is single-phase on either side and is thermodynamically stable relative to both PbO and TeO_2. Only when higher lead and tellurium oxides appear in the oxide film do reactions become possible in the semiconductor–oxide system, but in this case the components of the semiconductor should not be segregated at the interface in the elemental form.

The phase equilibrium diagram for the In–P–O system has a different structure (Fig. 1*d*). It contains the stable InP–$InPO_4$ line, but InP is not linked by stable lines with either phosphorus

¶ The possibility of formation of the compounds $CdTe_2O_5$ and $HgTe_2O_5$, the presence of which has been mentioned in a number of studies,[16–18] has not been taken into account in Fig. 1 for CdTe and HgTe.

oxides or with In_2O_3. The InP–interface formed under equilibrium conditions is also single-phase on either side. If the composition of the oxide layer differs from $InPO_4$, there is a possibility of the occurrence of chemical reactions between the support and the oxide layer, which probably results in the appearance of both indium and phosphorus in the elemental form in the region of the interface.

The phase equilibrium diagram for the Hg–Se–O system (Fig. 1*e*) is a mirror image of the analogous phase equilibrium diagram for Cd–Te–O. The HgSe–oxide interface is single-phase but is unstable relative to mercury oxide. Elemental mercury may appear at the HgSe–oxide interface as a result of chemical reactions between the support and HgO.

Similarly the phase equilibrium diagram for the Hg–Te–O system (Fig. 1*f*) is the mirror image of the corresponding diagram for the Ga–As–O system. In the region of the HgTe–oxide interface, the chalcogen is oxidised preferentially, while mercury remains in the elemental form. The HgTe–oxide interface is unstable, since the only stable line on the diagram is $HgTe–TeO_2$, linking HgTe to the oxide phases. It follows from the phase equilibrium diagrams that the reactions between the support and the oxide should lead to the enrichment of the HgTe–oxide interface in metallic mercury.

Thus, judging from the phase equilibrium diagrams for the III–V, II–VI, and IV–VI binary semiconductors, there is a possibility of different variants of the phase composition and thermodynamic stability on semiconductor–oxide interfaces.

No less interesting results have been obtained with the aid of phase equilibrium diagrams for semiconductor solid solutions. The first three-dimensional diagrams, consisting of tetrahedra, have been constructed for the $In_xGa_{1-x}As$ [19] and $Hg_{1-x}Cd_xTe$ [11,16] solid solutions. The methods used to construct such diagrams were supplemented by several important postulates compared with the methods used to construct the phase equilibrium diagrams for binary semiconductors.[11] Stable triangular planes in the three-dimensional diagram play the role of the stable lines in the two-dimensional diagram. Each apex of such a triangle must correspond to one of the phases of the test system, each side of the triangle represents a stable line of the phase equilibrium diagram, and at least one apex of the triangle is located on a face of the tetrahedron. All possible planes are considered and their stability is estimated from the calculated free energies ΔG.

As an example, Fig. 2 presents the phase equilibrium diagram for the Hg–Zn–Te–O system. We may note that, apart from the phase equilibrium diagrams for the Hg–Te–O and Zn–Te–O systems, the estimation of the form of the phase equilibrium diagrams for the Hg–Zn–O and Hg–Zn–Te systems was needed in order to construct the phase equilibrium diagram for the $Hg_{1-x}Zn_xTe$–O system. Such three-dimensional diagrams can be used to determine the phase composition of the solid solution–oxide interface. The phase composition profile is estimated from the points of intersection of the straight line connecting the solid solution to oxygen with the stable lines and planes of the phase equilibrium diagram. A definite compound corresponds to each such point. The phase composition profiles are presented for the diagrams considered. Such analysis can be carried out conveniently by considering the cross-section through the three-dimensional diagram along the plane connecting the binary compounds of the solid solution and oxygen.

The most interesting variants of such cross-sections are presented in Fig. 3. Analysis can be usefully begun with the thoroughly investigated Hg–Cd–Te–O system. In the oxidation of the $Hg_{1-x}Cd_xTe$ solid solutions, CdTe is initially oxidised (the $Hg_{1-x}Cd_xTe$–O straight line belongs to the stable HgTe–$CdTeO_3$–CdTe plane) (Fig. 3*a*). After the completion of the oxidation of CdTe (the $Hg_{1-x}Cd_xTe$–O straight line intersects the stable $HgTe–CdTeO_3$ line), the oxidation of HgTe begins with the preferential formation of the chalcogen in the initial stage, mercury being segregated in the elemental form at the interface.

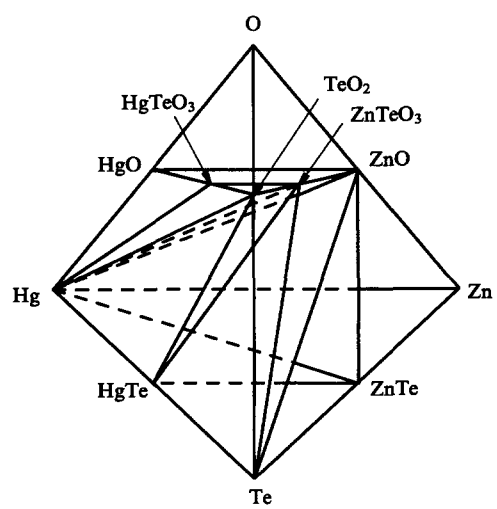


Figure 2. Phase equilibrium diagram for the Hg–Zn–Te–O system.[13]

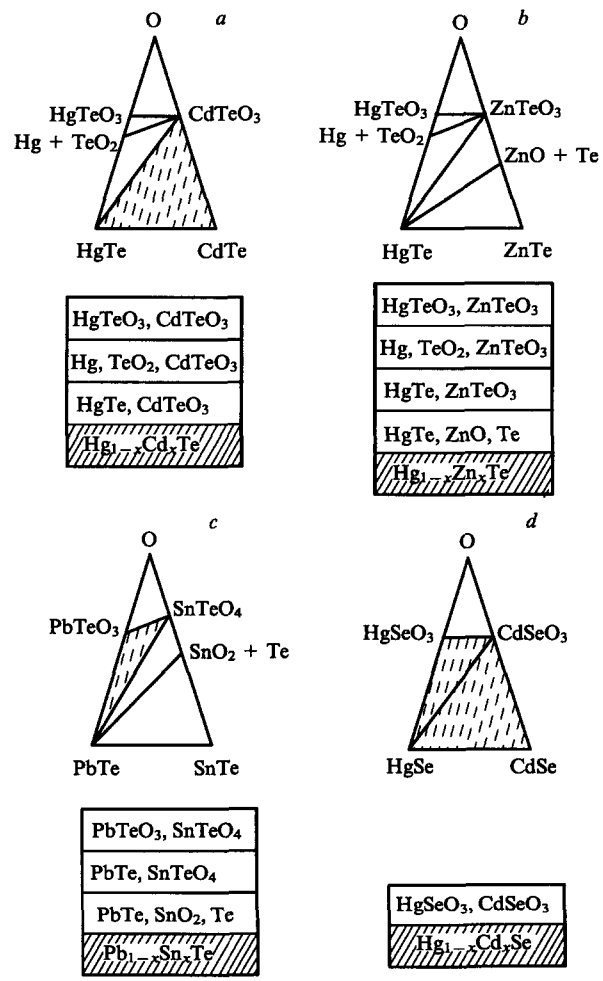


Figure 3. Sections through phase equilibrium diagrams for various systems:
(*a*) Hg–Cd–Te–O along the HgTe–O–CdTe plane;[11]
(*b*) Hg–Zn–Te–O along the HgTe–O–ZnTe plane;[13]
(*c*) Pb–Sn–Te–O along the PbTe–O–SnTe plane;.[12]
(*d*) Hg–Cd–Se–O along the HgSe–O–CdSe plane.[13]
The corresponding phase composition profiles for the intrinsic oxides are shown under the sections.

Thus the solid solution–oxide interface is multiphase and contains metallic mercury (Fig. 3*a*).

The opposite oxidation pattern is characteristic of the $Pb_{1-x}Sn_xTe$ solid solution (Fig. 3*c*). Here SnTe is oxidised first, giving rise to SnO_2 and elemental tellurium. Thus, in contrast to $Hg_{1-x}Cd_xTe$, the solid solution–oxide interface for $Pb_{1-x}Sn_xTe$ contains the elemental chalcogen.

An even more complex situation obtains for the $Hg_{1-x}Zn_xTe$ solid solution. Analysis of the HgTe–O–ZnTe section (Fig. 3*b*) shows that, in the oxidation of the $Hg_{1-x}Zn_xTe$ solid solution, ZnTe is the first to be oxidised with formation of ZnO and elemental tellurium [the $Hg_{1-x}Zn_xTe$–O line intersects the Hg–ZnO–Te plane (Fig. 2)]. Then tellurium is oxidised to zinc tellurite $ZnTeO_3$ (the $Hg_{1-x}Zn_xTe$–O line intersects the Hg–$ZnTeO_3$ line). Next, the oxidation of HgTe begins, tellurium being oxidised preferentially, and elemental mercury is evolved at the interface. Consequently the simultaneous presence of elemental tellurium and mercury in the region of the solid solution–oxide interface is characteristic of the $Hg_{1-x}Zn_xTe$ solid solution.

Analysis of the HgSe–O–CdSe section (Fig. 3*d*) shows that the $Hg_{1-x}Cd_xSe$ solid solution is unique. By virtue of the presence of the stable CdSe–$CdSeO_3$ and HgSe–$HgSeO_3$ lines on the phase equilibrium diagrams for the Cd–Se–O and Hg–Se–O systems, the corresponding HgSe–O–CdSe section represents a stable plane. The equilibrium oxidation of the $Hg_{1-x}Cd_xSe$ solid solution reduces to the oxidation of CdSe and HgSe to $CdSeO_3$ and $HgSeO_3$ respectively. Because of this, the solid solution–oxide interface should exhibit thermal stability. As regards other solid solutions considered above, the solid solution–oxide interface is multicomponent and thermodynamically unstable. In view of the absence of any stable planes in, for example, the HgTe–O–ZnTe section, the solid solution–oxide interface is multicomponent and potentially unstable. However, as will be shown below, this multicomponent property has a mutually compensating character (Hg^0 and Te^0) and paradoxically can actually improve the properties of the interface.

Similar phase equilibrium diagrams can also be constructed for even more complex systems. For example, the phase diagram for the $(PbSe)_{1-x}(SnTe)_x$ four-component solid solution has been published.[20] It was shown that in this system both chalcogens are present as a phase in thermodynamic equilibrium in the region of the solid solution–oxide interface.

The method of phase equilibrium diagrams can be employed also for the analysis of the processes occurring when a metal is deposited on the oxidised surface of a semiconductor.[21]

Fig. 4 presents as an example the phase equilibrium diagram for the Pb–Te–O–Al system. Analysis of sections through this diagram along the PbTe–O–Al plane makes it possible to estimate the phase composition of the PbTe–Al interface depending on the initial chemical state of the semiconductor surface. The composition of the PbTe surface is represented along the base of the PbTe–O–Al triangle by a point the movement of which, within the limits of the PbTe–$PbTeO_3$ segment, corresponds to the change in the state of the surface from that of a completely unoxidised semiconductor to a continuous oxide film. When aluminium is deposited on the unoxidised PbTe surface, chemical interaction takes place, which results in the formation of Al_2Te_3 and metallic lead (when the PbTe–Al straight line is drawn, it intersects the stable Al_2Te_3–Pb line). When aluminium is deposited on an oxidised PbTe surface, it initially interacts with the oxide, which results in the formation of Al_2O_3 and PbTe and then (depending on the thickness of the oxygen layer) it interacts with the semiconductor support or with the products of the first reaction. If the point on the PbTe–$PbTeO_3$ segment is connected with the apex of the PbTe–O–Al triangle, then the straight line is initially located in the PbTe–$PbTeO_3$–Al_2O_3 plane and then intersects the Pb–Al_2Te_3–Al_2O_3 plane. Thus, when aluminium is deposited on the oxidised PbTe surface, chemical interaction between the metal and the oxide is to be expected. This results in a decrease in the thickness of the oxide film and in the formation of

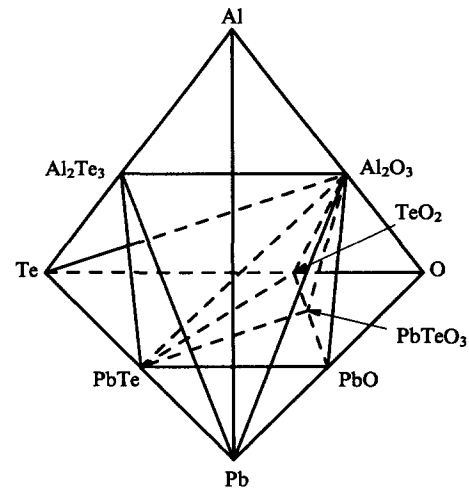


Figure 4. Phase equilibrium diagram for the Pb–Te–O–Al system.[21]

a boundary layer containing Al_2O_3, Al_2Te_3, and metallic lead and there is a possibility of the complete disappearance of the initial oxide.

It has been observed experimentally that different variants of the sulfidation † of the surfaces of semiconductors greatly improve their electrophysical properties. Phase equilibrium diagrams were constructed for certain semiconductor–sulfur systems (Fig. 5). None of them differ fundamentally from the phase equilibrium diagram for the Ga–As–O system, i.e. in this case the elemental nonmetal phase is formed at the semiconductor–sulfide interface. At the same time, the phase equilibrium diagram for the In–P–S system contains the stable InP–In_2S_3 line, while the phase equilibrium diagram for the Ga–As–S system contains the stable GaAs–GaS line, i.e. in each system there is a sulfide and the interface between the latter and the semiconductor is thermodynamically stable. An exchange reaction takes place in the Cd–Te–S and Hg–Te–S systems (Fig. 5*c*).

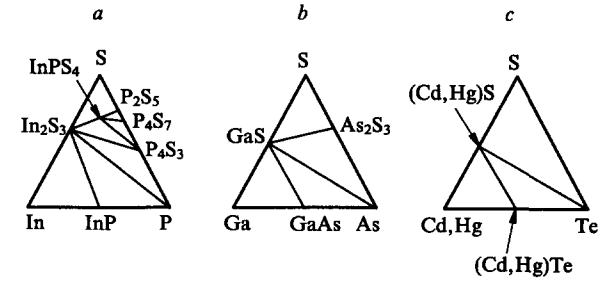


Figure 5. Phase equilibrium diagrams for different systems: (*a*) In–P–S;[22] (*b*) Ga–As–S;[23] (*c*) (Cd,Hg)–Te–S.[24]

Useful information about the composition and thermodynamic stability of the intrinsic insulator has been obtained with the aid of the phase equilibrium diagram for the $Hg_{1-x}Cd_xTe$–F system.[24] It was established that, as in the sulfidation of the III–V semiconductors, in the fluorination of CdTe at the CdTe–CdF_2 interface the elemental nonmetal is evolved and the CdTe–CdF_2 line is thermodynamically stable. On the other hand,

† The problem of the sulfidation of the surfaces of III–V semiconductors is one of the crucial problems in semiconductor materials science at the present time. We shall be concerned only with those aspects of the problem which are linked directly with the aim of this review.

on fluorination of HgTe the liberation of the components of the material in the elemental form should not be observed at all. Comparison of the sections through the Hg–Cd–Te–F diagram along the HgTe–F–CdTe plane, through the Hg–Cd–Te–S diagram along the HgTe–S–CdTe plane,[24] and through the Hg–Cd–Te–O diagram along the HgTe–O–CdTe plane (Fig. 3*a*) permits the conclusion that the principal feature of the $Hg_{1-x}Cd_xTe$–intrinsic insulator interface in the sulfidation and fluorination reactions is the absence of elemental mercury. On the other hand, the phase equilibrium diagram predicts the liberation of the elemental chalcogen in both cases. Its amount in the fluorination reaction should be significantly smaller, since the source of Te^0 is only CdTe, the content of which does not exceed 30% in the compositions of the $Hg_{1-x}Cd_xTe$ solid solution of the greatest practical importance.

It will be shown below whether the differences in the phase equilibrium diagrams presented above lead to different properties of the MIS materials based on these systems.

III. Experimental data on the oxidation of semiconducting compounds

Thin oxide films ($\leqslant 5$ μm) are used in semiconductor electronics, the thickness becoming continuously smaller with progress in the technology. For example, in modern MOS transistors the thickness of the oxide under the gate is ~25 nm. The composition of the semiconductor–oxide interface itself, whose thickness in most cases does not exceed several nanometers, is of greatest interest to investigators. This must be borne in mind in comparing the chemical compositions of the oxide films predicted by the phase equilibrium diagram and obtained experimentally.

Electronic and ionic spectroscopic methods, which make it possible to investigate the composition and structure of the surface and interfaces at the atomic level, are usually employed in the study of such oxide films.[25] In the first place these are methods, such as electronic Auger spectroscopy (EAS) combined with ionic etching, which make it possible to determine the distribution of the elements in the bulk of the structure. The particles of the specimen atomised by the primary ionic beam are analysed by secondary ion mass spectrometry (SIMS). The Rutherford back scattering (RBS) method has almost no disruptive effect, but is resolution as a function of depth is poorer.

Photoelectron spectroscopy (PES) affords the most valuable information about the chemical bonds linking the elements on the surface and the interface. Ultraviolet (UPES) and X-ray photoelectron spectroscopy (XPES) are distinguished by the energy range of the primary radiation beam.

Valuable information, particularly in the presence of Group V and VI nonmetals, has also been obtained with the aid of Raman spectroscopy and the voltammetric method.

For the purpose of analysis, it is convenient to divide the theoretical and experimental results into three groups depending on the oxidation conditions: 'natural' oxidation (at room temperature), thermal oxidation, and anodic electrochemical oxidation (photochemical oxidation and oxidation in an oxygen plasma are also usually included here). One should bear in mind that, for each of these oxidation procedures, there exist technological factors which lead to the deviation of the composition of the oxide films from the equilibrium composition — for example, thermal decomposition in thermal oxidation, different solubilities of the oxide phases in the electrolyte in anodic oxidation, etc. Only correct allowance for these factors makes it possible to achieve a correct comparison.

1. Gallium arsenide

The natural oxidation processes were initially investigated mainly on chemically etched surfaces, but the results obtained by different investigators proved to be extremely contradictory; this was associated primarily with the fact that etching can appreciably disturb the stoichiometry of the surface. In addition, oxidation is a component of the etching process which leads to the growth of insoluble oxide films of different composition depending on the composition of the etch. This has been demonstrated clearly for the InP surface.[26] According to data obtained by the XPES and RBS methods, the thickness of the grown oxide layer varied from 0.7 to 2.4 nm depending on the composition of the etch and the etching time, while the ratio of phosphorus and indium, normalised with respect to $InPO_4$, ranged from 0.2 to 1.5. Similar results have been obtained from GaAs[27] and $Hg_{1-x}Cd_xTe$.[18]

This is why the study of the oxidation of an atomically clean surface (ACS), usually obtained by cleaving the crystal in an ultrahigh vacuum or by ion bombardment, is of greatest interest. Electron spectroscopy makes it possible to observe the oxygen adsorption process at the monolayer level on such a surface. However, one should bear in mind that the thickness of the oxide, growing on the ACS of III–V and II–VI compounds, does not usually exceed 2–3 monolayers, i.e. it is too small to permit a description of these films by means of the thermodynamic parameters obtained for bulk phase specimens. Furthermore, the differences between the electronic and lattice subsystems of the atomic layers on the free surface and in the parallel layers in the bulk of the semiconductors are particularly strongly manifested precisely in the initial stages of the interaction of oxygen with the semiconductor.[28] These differences actually explain, for example, the finding that, when the ACS on silicon was oxidised for an oxide thickness of ~1 nm, unstable oxidation states of silicon were observed by the UPES method.[1]

Despite these limitations, it is possible to establish a definite relation between the phase equilibrium diagram and the oxidation of the ACS of semiconductors at room temperature. It has been established with the aid of electronic spectroscopy that the unexcited oxygen molecules interact with the surface of GaAs, InAs, and InP in three stages.[29–32] Adsorption takes place in the first stage but only on surface defects formed on cleavage or on cleaning the surface by ion bombardment. In the second stage, the oxygen molecule dissociates with formation of bridge bonds of the Ga–O–As type. The interaction accompanied by a chemical shift of the skeletal levels begins only in the third stage. For all three compounds, the atoms of both the metal and the nonmetal participate equally in the formation of bonds with oxygen, since the amplitude of the PE peaks due to oxidised indium (gallium) and arsenic (phosphorus) increases equally with increase in the surface coverage by oxygen in the range from 0.1 to 1.5 monolayers.[32,33] However, after brief annealing of InP in vacuo at 350 °C, the PE peaks for indium, phosphorus, and oxygen remain unchanged, whereas after annealing GaAs the peak for oxidised gallium increases and that for oxidised arsenic diminishes while the amplitude of the oxygen peak remains unchanged.

According to the phase equilibrium diagrams (Fig. 1), the oxide layer on InP consists of the compound $InPO_4$, which is stable on heating, while that on GaAs comprises a mixture of oxides,[34] the heating of which gives rise to the reaction

$$2GaAs + As_2O_3 = Ga_2O_3 + 4As. \quad (1)$$

On the other hand, on oxidation of the ACS on gallium arsenide by ionised oxygen, the chemical interaction is accelerated (peaks corresponding to Ga_2O_3 and As_2O_3 appear in the photoelectron spectrum) and a peak corresponding to elemental arsenic appears.[29] The appearance of elemental antimony has been observed in the oxidation of the ACS of gallium and indium antimonides.[35,36] The difference between even the initial stages of the oxidation of GaAs and InP is indicated by the analysis of the composition of thin ‡ layers obtained by the natural, chemical, and thermal oxidation of GaAs and InP specimens.[37,38] All the

‡ Thin layers are understood as layers whose thickness is comparable to the depth from which photoelectrons emerge (< 5 nm). Their composition, like that of the interface, can be analysed in depth without resorting to etching.

specimens were subjected to the same preliminary surface treatment and the composition was investigated by the XPES method with angular resolution, which makes it possible to vary the depth of the probed layer from 2 to 4 nm. Both elemental arsenic and gallium and arsenic suboxides were observed in all the oxide layers on GaAs under these conditions, whereas both elemental phosphorus and indium and phosphorus suboxides were absent from the oxidised InP surface and the entire oxidised phosphorus was present in the form of complex compounds.

Studies on the thermal oxidation of GaAs (see Wilmsen's review[39]) showed that elemental arsenic is present on the interface under different annealing conditions (dry and moist oxygen, O_2/As_2O_3 mixture) over a wide temperature range ($\leqslant 620$ °C). Only at higher temperatures does its concentration diminish and $GaAsO_4$ appears on the interface in addition to Ga_2O_3. The oxide layer at $T \leqslant 500$ °C consists largely of amorphous Ga_2O_3, which crystallises as β-Ga_2O_3 at higher temperatures; As_2O_3 is present in much smaller amounts. This is associated both with the consumption of As_2O_3 via reaction (1) and with its high volatility. The concentration of As_2O_3 in the bulk phase can be increased by growing the oxide in the vapour of As_2O_3 or the O_2/As_2O_3 mixture. The exact spatial disposition of arsenic remained unelucidated for a long time. It was assumed that it may accumulate in the form of a continuous film directly on the interface. However, the latest studies have shown that elemental arsenic is present throughout the bulk of the thermal oxide,[40] while analysis of the cross-sections through structures with the thermal oxide with the aid of transmission microscopy and microdiffraction confirmed that, for example after oxidation at 500 °C, the interface consists of an epitaxial layer of γ-Ga_2O_3 on GaAs, beween which are injected 5–10 nm precipitates of hexagonal arsenic with a density of $(2-5) \times 10^{11}$ cm^{-2}.[41] In addition, it was shown that arsenic may be formed not only in reaction (1) but also in the direct GaAs oxidation reaction

$$4GaAs + 3O_2 = 2Ga_2O_3 + 4As, \quad (2)$$

first put forward by Smirnova et al.[42]

One of the controversial questions is whether elemental arsenic is or is not formed at the interface in the low-temperature oxidation (electrochemical anodic, plasma, etc. oxidation). The majority of investigators believed that it appears at the interface only after the annealing of the grown oxides at $T > 250$ °C as a result of a secondary reaction. However, it was later shown[42] that As^0 could not be detected in the initial film as a consequence of the inadequate sensitivity of the Raman technique ($\sim 10^{15}$ atoms cm^{-2}). Thus, when solid-phase voltammetry having a sensitivity of $10^{11}-10^{12}$ atoms cm^{-2} was used, it was possible to detect elemental arsenic and antimony in the initial anodic oxide films (AOF) on GaAs, InAs, and InSb,[5,40,42] i.e. reaction (1) occurs also at room temperature under these conditions. Furthermore, it has been possible to carry out a layer-by-layer investigation using this method of not only the phase composition but also of the structure of the oxide layers and to establish its relation with the conditions governing the growth of the anodic oxide.[42]

Thus the anodic oxide film, approximately 100 nm thick, grown under galvanostatic conditions ($j \approx 5.0$ mA cm^{-2}) on the GaAs surface, has the following distribution of composition as a function of its thickness:[40]

Layer	Chemical composition
1	ε-Ga_2O_3, As_2O_3(cryst.), As_2O_3(amorph.), $GaAsO_4$(cryst.)
2	ε-Ga_2O_3, As_2O_3(amorph.), As_2O_3(cryst.), As_2O_5(cryst.), As_2O_4(cryst., traces)
3	α-Ga_2O_3, ε-Ga_2O_3, As_2O_3(amorph.), As_2O_5(cryst., traces)
4	α-Ga_2O_3, As_2O_3(amorph.), As_2O_5 (cryst., traces)
5	δ-Ga_2O_3, As_2O_3(cryst.), As(amorph.), As(cryst.)

Layer 5 adjoins the GaAs surface. Evidently, Ga_2O_3, As_2O_3, and As are formed at the interface, which agrees with the phase equilibrium diagram. On moving away from the interface, oxides appear in which arsenic has the highest oxidation state (As_2O_4, As_2O_5, $GaAsO_4$), and the nonequilibrium combinations of phases $As_2O_3 + As_2O_5$, and $Ga_2O_3 + As_2O_5$ are observed, which is most probably associated with kinetic factors. After a time or on heat treatment, this leads to the following solid-phase reactions:

$$As_2O_3 + As_2O_5 = 2As_2O_4, \quad (3)$$

$$Ga_2O_3 + As_2O_5 = 2GaAsO_4, \quad (4)$$

$$Ga_2O_3 + 2As_2O_4 = 2GaAsO_4 + As_2O_3. \quad (5)$$

Under these conditions, structural transformations also occur in the films — the amorphous forms of As and As_2O_3 crystallise and the less stable crystalline forms of Ga_2O_3 are converted into the more stable ones. The chemical state is in many respects determined by the conditions in the anodic oxidation.[40,43] Thus an increase in current density leads to additional oxidation of arsenic to the pentavalent state and to the appearance of As^0 at the interface in both amorphous and crystalline forms. Comparison of the spectra of the analytical signals due to the electrochemical transformations of the anodic oxide, the thermal oxide, and mixtures of reference compounds shows that none of these oxides are homogeneous, consisting of a mixture of phases of different structural modifications with a grain size greater than 5 nm.[40] This agrees well with the existing data showing that the oxides are initiated in isolated regions on exposure to an electron beam[44] and in the initial stages of the growth of the anodic oxide.[45]

The chemical composition of the oxide layer on GaAs, obtained by oxidation in an oxygen plasma,§ does not actually differ from the composition of the layer obtained on anodic oxidation and also represents a mixture of As_2O_3 and Ga_2O_3. Its composition is then influenced quantitatively by factors such as the rate of growth of the oxide, the degree of ionisation of the plasma, and the anodic current density. The concentration of arsenic in the plasma oxides is found to be higher than in the electrochemical oxides and can reach 4%–5% of the overall composition.[47] It is determined to a large extent by the dynamics of the growth of the oxide layer: the more intense the oxidation process, the smaller the amount of arsenic displaced to the interface. Its total amount at a high rate of growth (300 nm min^{-1}) is equivalent to a layer 4.2 nm thick, while at a low rate of oxidation it corresponds to 41 nm for an overall thickness of the layer of 160 nm.[48] One cannot rule out the possibility that the appearance of such a large amount of elemental arsenic is associated with the preferential oxidation of gallium as a consequence of the difference between the activation energies for the gallium and arsenic oxidation reactions in the plasma.[49]

2. Indium phosphide

XPES analysis of thin oxide films grown under an oxygen atmosphere at temperatures in the range 340–400 °C showed that they are a mixture of amorphous In_2O_3 and $InPO_4$ and that phosphorus is present as the phosphate and not P_2O_5 over the entire experimental temperature range (up to 650 °C), but, with increase in the oxidation time, i.e. for thicker films, elemental phosphorus appears at the interface.[39] With increase in the oxidation temperature from 350 to 550 °C, the amount of accumulated P^0 increases and then falls.[50] At ~ 650 °C, elemental phosphorus was not detected[39] and only $InPO_4$ was found at the interface, which is consistent with the phase equilibrium diagram. The appearance of P^0 is probably associated with the fact that at $T < 600$ °C the oxide grows as a result of the diffusion of indium and phosphorus to the oxide surface, the diffusion of phosphorus being appreciably slower than that of indium. The extent of the

§ The preparation of the oxides of compound semiconductors by plasma anodisation and their properties have been described in detail.[46]

diffusion of oxygen at these temperatures is low and the oxidation occurs on the surface, which in fact leads to the accumulation of unoxidised phosphorus at the interface. Furthermore, according to Mittova et al.,[51] unoxidised (or insufficiently oxidised) indium is formed in the bulk of the oxide during thermal oxidation at 575–675 °C. On the other hand, in general the excess indium present in the thermal oxide on InP, especially in the outer layer, is due to the evaporation of phosphorus from the surface.[52] Thus, in a certain temperature range, kinetic factors become dominant. Experiments on the oxidation of InP at oxygen pressures in the range from 1 to 500 atm confirmed that this is in fact so and that the appearance of P^0 is not associated with the reactions of types (1) and (2). At pressures of 150 atm and above, the interface consists of $InPO_4$, In_2O_3, and P_2O_5. Such a change in the composition of the interface can be explained by the increase in the rate of diffusion of oxygen, which in fact leads to the complete oxidation of the elements.[53] It is of interest to note that P^0 is not formed on oxidation of InP by oxygen in the presence of water vapour.[39]

A detailed comparison of the elemental compositions of the thermal, chemical, and anodic oxides of InP has been carried out with the aid of XPES using precision layer-by-layer chemical etching, which ruled out all the effects associated with the action of the ion beam.[50, 54–56] A sufficiently reliable identi-fication of different oxide phases was achieved by comparing the chemical shifts of the peaks for different levels of the skeleton, their intensities, and the spectra of the valence bands of the oxide films and reference compounds. If the thermal oxides represent a mixture of amorphous In_2O_3 and $InPO_4$ particles with the P^0 present at the interface, then they also include polyphosphates of the type $In(PO_3)_x$. The oxides grown in concentrated nitric acid under strong illumination are homogeneous throughout their thickness. Their average atomic composition corresponds to $In(PO_3)_{2.6}$ and is independent of the thickness of the oxide layer, time, and the temperature ($\leqslant 80$ °C) of the growth process. Anodic oxides have been grown in the familiar AGW electrolyte,[57] the pH of which was varied in the range from 2 to 12 by adding NH_4OH. They all consist of two layers, the outer layer being enriched in indium (P : In = 0.4) and representing apparently a hydrated mixture of $InPO_4$ and In_2O_3 or $In(OH)_3$. The inner layer, adjoining the interface, is enriched in phosphorus and has the average composition $In(PO_{3.2})_{3.9}$. This distribution remains unchanged for all anodic oxides with a thickness between 10 and 50 nm and is independent of both the pH of the electrolyte and the current density. The distributions of the elements in the anodic oxide and in the oxides grown in other electrolytes[58, 59] are quantitatively the same. This has been attributed to the growth mechanism specific for the anodic InP oxide, which cannot operate in, for example, GaAs, because the anodic oxide on GaAs is not a vitreous compound but a mixture of polycrystalline oxides.

Analysis of the photoelectron spectra of the valence band has shown that the inner part of the anodic oxide on the side of the interface consists of single-phase nonstoichiometric phosphate $In(PO_x)_y$ with x and y close to 3. Studies by the fast electron diffraction method showed that the oxides are amorphous. This agrees with the existence of vitreous $In(PO_3)_3$.[60] The study of the crystalline metaphosphate $In(PO_3)_3$ showed that the P–O–P bond angle in the PO_4 tetrahedron can vary within wide limits, like the O–Si–O angle in the SiO_2 structure, i.e. these structures are sufficiently flexible to ensure a good agreement between the phosphate and InP lattices, as happens in the Si–SiO_2 system. Annealing at temperatures up to 350 °C does not alter the chemical composition of the anodic oxide or of the interface with InP and, furthermore, according to data obtained by transmission electron microscopy, somewhat smoothes out the roughness of the interface at the atomic level. The change in the composition of the interface (the formation of a P^0 layer up to 0.5 nm thick) is observed only after annealing at 450 °C. The appearance of phosphorus can be explained, in conformity with the phase equilibrium diagram (Fig. 1*d*), by the fact that the InP–anodic oxide interface is nevertheless unstable and the reaction

$$4In(PO_3)_3 + 5InP = 8P + 9InPO_4, \quad (6)$$

takes place on it. One cannot rule out the possibility that, as a consequence of the presence of hydrates in the anodic oxide layer, additional reactions take place at high temperatures and result in the liberation of phosphorus.

An oxide consisting mainly of a polymeric polyphosphate phase has been obtained on indium phosphide by plasma oxidation.[61]

3. Semiconductor solid solutions

A few studies have shown that the oxidation reactions of solid solutions of III–V compounds can be regarded as a superposition of the oxidation reactions of the binary semiconductors. The appearance of a new As_zP_{1-z} phase in the oxidation of the $InAs_xP_{1-x}$ solid solution may be regarded as the most interesting result.[62]

It is noteworthy, in connection with the widescale use of $Hg_{1-x}Cd_xTe$ (x = 0.2, 0.3) and $Pb_{1-x}Sn_xTe$ (x = 0.2) in IR techniques, that mainly the solid solutions have been investigated, whereas the initial binary compounds HgTe and CdTe, as well as PbTe and SnTe, were considered only for a better understanding of the oxidation reactions of the solid solutions.

The study of the oxidation of the ACS of epitaxial $Pb_{1-x}Sn_xTe$ (x = 0, 0.2, and 1.0) showed that[63] SnTe is oxidised much more vigorously than PbTe. The rapid oxidation of tin is also characteristic of the solid solution and is accompanied by the enrichment of the surface in this element as a result of the sublimation of free tellurium. Vacuum annealing leads to the complete transition of tin to the oxidised state and hence to a decrease in the XPES peak associated with TeO_2. Bearing in mind the low temperature of the sublimation of elemental tellurium, the experimental data are seen to agree well with the phase equilibrium diagram (Fig. 3*c*).

The oxidation of the ACS of HgTe and $Hg_{0.7}Cd_{0.3}Te$ begins with the rupture of the Hg–Te bonds and the subsequent oxidation of tellurium but not mercury, the atoms of which leave the surface of this semiconductor, while both elements are oxidised in CdTe.[64] Comparison of the kinetics of the oxidation of all three materials showed that the solid solution is not oxidised as a simple mixture of two binary compounds. This can be explained by the fact that, on formation of the solid solution, a charge redistribution takes place between the mercury and cadmium ions and leads to the weakening of the Hg–Te bonds and to the strengthening of the Cd–Te bonds.[65]

Thermal oxidation has been investigated only for CdTe in view of the low thermal stability of mercury chalcogenides.[66] According to AES and XPES data, the thermal oxide, grown in both dry and moist oxygen at temperatures in the range 350–500 °C, consists of $CdTeO_3$ and no traces of enrichment of the interface in cadmium or tellurium were found. Furthermore, electron diffraction data show that epitaxial layers of cubic $CdTeO_3$ grow on CdTe at these temperatures. Complex cadmium and mercury oxide compounds are also present in the $Hg_{1-x}Cd_xTe$ oxides.[67]

Among all the variants of the oxidation reaction used to protect the $Hg_{1-x}Cd_xTe$ surface, anodic oxidation, carried out in 0.1 M KOH solution in 9 : 1 ethylene glycol–water mixture at a current density of 0.3 mA cm^{-2} under galvanostatic conditions, has unquestionably been most thoroughly investigated.[68] The composition and mechanisms of the growth of the anodic oxide have been studied by various methods. Fairly contradictory results have been obtained. At the present time, one can regard it as reliably established[69, 70] that the anodic oxide on $Hg_{1-x}Cd_xTe$ grows at the semiconductor–oxide interface as a result of the interaction of the atoms of the oxide with oxygen migrating to the interface via a vacancy mechanism. Oxygen vacancies migrate under the influence of the electric field in the direction towards the

outer boundary of the anodic oxide. At the oxide–electrolyte interface, the vacancies are filled with oxygen as a result of the electrochemical reaction. At this boundary, the oxide only dissolves in the electrolyte but does not grow.

Taking into account the available experimental data, the following model of the $Hg_{1-x}Cd_xTe$–anodic oxide interface has been proposed (Fig. 6*a*).[71,72] The $CdTeO_3$ layer is in direct contact with the semiconductor. The layer is formed because the binary components of the solid solution of CeTe and HgTe are oxidised separately — CdTe is oxidised preferentially, while HgTe remains partly unoxidised (private communication by Seelmann-Eggebert and H Richter — see Stahle et al.[73]). The anodic oxide grows into the semiconductor support, while the unoxidised HgTe remains in the layer adjoining the interface. The oxygen concentration is higher here, so that gradual further oxidation of HgTe takes place. In the bulk of the anodic oxide, all the components are fully oxidised and it is homogeneous as regards elemental composition. Comparison of the elemental composition determined experimentally by different methods with the composition calculated on the assumption that the entire oxidised semiconductor has been converted into a stoichiometric mixture of $HgTeO_3$ and $CdTeO_3$ has shown that more mercury than tellurium dissolves during the anodic oxidation. The anodic oxide has the following phase composition: 52% $HgTeO_3$, 30% TeO_2, and 18% $CdTeO_3$.[72] It is fully amorphous with the exception of the layer at the interface, where 2–5 nm crystalline particles are encountered. They have been identified as particles of unoxidised HgTe.

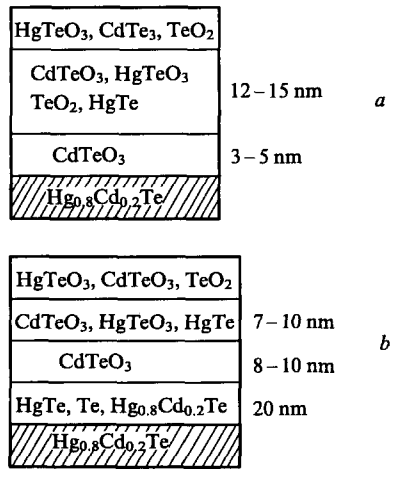


Figure 6. Phase composition profiles for the anodic oxide on $Hg_{0.8}Cd_{0.2}Te$: (*a*) after growth (before annealing; (*b*) after annealing at 220 °C.[72]

Annealing at relatively low temperatures (150 °C and above) leads to an appreciable redistribution of the elements at the interface, primarily to a decrease in the cadmium content in the semiconductor and an increase in its content of the oxide, the change in the composition involving HgTe being of the opposite kind.[71] This is unquestionably associated with the thermodynamic instability of the $Hg_{1-x}Cd_xTe$–oxide interface (Fig.3*a*). However, in the model illustrated in Fig. 6*a* the interface itself is thermodynamically stable, since $Hg_{1-x}Cd_xTe$ is in contact only with $CdTeO_3$, which is thermodynamically stable, and with HgTe and CdTe (continuous lines in Fig. 3a). It has therefore been suggested[72] that the $CdTeO_3$ layer in too porous and thin to prevent the interaction of TeO_2 with $Hg_{1-x}Cd_xTe$:

$$3TeO_2 + 10Hg_{0.8}Cd_{0.2}Te = 2CdTeO_3 + 8HgTe + 3Te. \quad (7)$$

This leads to some thickening of the $CdTeO_3$ layer and to the appearance of mercury telluride and tellurium in the semiconductor support (Fig. 6*b*). However, no account is taken of the possibility of the appearance of metallic mercury at the interface either directly during the period of oxidation or during subsequent heating as a consequence of a whole series of other thermodynamically feasible reactions, for example the interaction of $HgTeO_3$ with $Hg_{1-x}Cd_xTe$. However, in the presence of metallic mercury, it is impossible to account for the change in the electrical properties of the $Hg_{1-x}Cd_xTe$ surface layer (protected by the anodic oxide) during annealing.[71,74–76] According to RBS data, an appreciable increase in the mercury content after annealing at 200–250 °C is observed in the surface layer of the semiconductor approximately 20 nm thick.[76] The concentration of excess mercury under these conditions is up to 2×10^{21} cm^{-3}. Part of the mercury is actually segregated as HgTe, which alters the composition of the surface layer of the solid solution (according to optical absorption spectra, x diminishes to 0.125). The remainder accumulates in the form of mercury atoms in the interstices, which diffuse into the bulk of the semiconductor during annealing.

As in the case of GaAs and InP, the plasma oxide on $Hg_{1-x}Cd_xTe$ does not differ from the anodic oxide either as regards composition or the structure of the interface.[77] On the other hand, depending on the process conditions during photochemical oxidation, the compositions of both the oxide itself and of the interface, in particular their depletion or enrichment in mercury, can vary within wide limits. This is associated with the complexity of the oxide growth mechanisms.[78] Furthermore, it has been shown in relation to the photochemical oxide how greatly the composition of the interface for a compound semiconductor may depend on the preliminary treatment of the oxidised surface.[18]

An AES study of the anodic oxide on PbTe showed[79] that the distributions of the metal and the chalcogen in it agree fully with the distributions of cadmium and tellurium in the CdTe oxide.[67] This can be attributed to the fact that in both cases oxidation leads to the formation of the tellurite. RBS data indicate that the oxygen content in the bulk of the anodic oxide corresponds to lead in the Pb^{4+} oxidation state and not to Pb^{2+}, i.e. the appearance of the higher lead oxides — PbO_2 or $PbTeO_4$ — in the final stages of the oxidation reaction, predicted on the basis of the phase equilibrium diagram, has been confirmed experimentally for PbTe.

Comparison of the distributions of the elements at the oxide–semiconductor interface for the oxides on $Pb_{0.8}Sn_{0.2}Te$, obtained by the anodic,[80] plasma,[81] chemical,[82,83] and thermal[84] oxidation, yields interesting results. It shows that, although the compositions in the bulk of the oxides and especially in their outer layer differ appreciably, all the characteristics of the interface, which are already manifested on natural oxidation and, as stated above, are associated with the preferential oxidation of tin, are retained and actually intensify for all the oxidation methods. This concerns primarily the redistribution of tin and lead at the interface, which has been observed[85] in the oxidation of Pb–Sn alloys and which can be explained by topochemical substitution reactions typical for the initial stages of the oxidation of binary alloys of metals with different oxygen affinities.[86] However, also the appearance of elemental tellurium should be observed in the oxidation of tellurides (Fig. 3*c*).

Studies by Raman spectroscopy have made it possible to detect Te^0 on the naturally oxidised surface of only SnTe.[87] For $Pb_{0.8}Sn_{0.2}Te$, elemental tellurium can be detected only after thermal oxidation at $T \geqslant 250$ °C. For the anodic oxide on $Pb_{0.8}Sn_{0.2}Te$, elemental tellurium is also detected after annealing at this temperature. As in the case of As^0 in GaAs, its appearance here is associated primarily with the thermodynamically favourable secondary process

$$SnTe + TeO_2 = SnO_2 + 2Te. \quad (8)$$

At the same time, elemental tellurium could not be detected in the chemical oxide even on annealing. This is apparently associated with the characteristic features of the growth of the oxide film by this method.[83] The oxide always contains unoxidised PbTe, which

accumulates, in combination with SnO_2, at the interface, ensuring its thermodynamic stability.

Electrochemical anodisation has been used successfully to produce on the $Hg_{1-x}Cd_xTe$ surface other intrinsic insulators—sulfides[88] and fluorides.[89] The process is in both cases similar to anodic oxidation and is carried out respectively in Na_2S and KF + KOH solutions in ethylene glycol. During the growth of the anodic sulfide, HgS and TeS_2 are dissolved preferentially. The growing layer consists of 30% HgS and 70% CdS with some excess of tellurium in the form of hexagonal ~5 nm particles.[90] The $Hg_{1-x}Cd_xTe$–anodic sulfide interface is sharp and the change in composition is observed at appreciably higher annealing temperatures than for the anodic oxide (350 °C for annealing in air in the course of 15 days). The changes are mainly associated with the evaporation of mercury.[91]

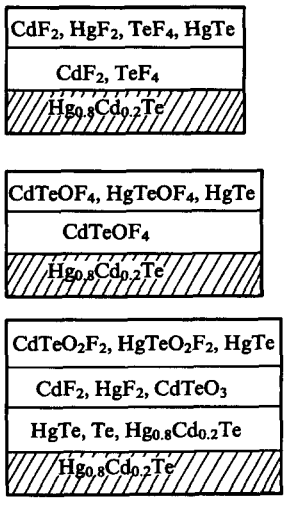


Figure 7. Phase composition profiles for the anodic fluoride on $Hg_{0.8}Cd_{0.2}Te$: (*a*) after growth; (*b*) after storage in air at room temperature; (*c*) after annealing at 220 °C.[92]

The study of the composition of the anodic fluoride on $Hg_{1-x}Cd_xTe$ showed,[92,93] that it consists mainly of 14% CdF_2, 21% HgF_2, 35% TeF_4, and 30% HgTe, i.e. the entire HgTe is not fluorinated. It is very significant that the interface is depleted in mercury fluoride and actually consists of only CdF_2 and TeF_4 (Fig. 7*a*). This should have promoted the thermal stability of the $Hg_{1-x}Cd_xTe$–anodic fluoride interface, but it has been found that the anodic fluoride is so sensitive to the presence of oxygen that oxide fluorides are formed even at room temperature (Fig. 7*b*). On heating, they react further with oxygen, which leads to the loss of fluorine:

$$2MTeOF_4 + O_2 = 2MTeO_2F_2 + 2F_2, \qquad (9)$$

where M = Hg or Cd. A reaction similar in many respects to that occurring in the annealing of the anodic oxide on $Hg_{1-x}Cd_xTe$ takes place at the interface, i.e.

$$3MTeO_2F_2 + 10Hg_{0.8}Cd_{0.2}Te = \\ = 3MF_2 + 2CdTeO_3 + 8HgTe + 3Te, \qquad (10)$$

which results in the formation of a multiphase interface similar to the $Hg_{1-x}Cd_xTe$–anodic oxide interface. It must be emphasised that the formation of metallic mercury is characteristic of only the $Hg_{1-x}Cd_xTe$–anodic oxide interface. As will be shown below, this is responsible for the fundamental differences between the electrophysical properties of these interfaces.

Owing to the instability of the anodic fluoride on $Hg_{1-x}Cd_xTe$ in the presence of not only oxygen but also water vapour, it is essential to provide additional protection to the anodic fluoride in practical applications, for example, by depositing ZnS.[94] Here it is necessary to take into account the possibility of chemical interaction between these compounds, leading to the appearance of ZnF_2, HgTe, and Te. When the anodic fluoride is sufficiently thick, its interaction does not affect the properties of the interface.

Similar chemical reactions, leading to partial reduction of the components of the anodic oxide on $Hg_{1-x}Cd_xTe$, occur also when ZnS[95] or metals (indium,[96] platinum, and gold[97]) are deposited on it. This must be taken into account in selecting the optimum thickness of the intrinsic insulator.

The knowledge of the possible chemical interactions in the semiconductor, the oxide, and the metal (Fig. 4) makes it possible to regulate specifically the properties of the metal–semiconductor interface with the aid of a thin intervening layer of oxide having a specified composition. Thus, by employing the chemical oxide, it has been possible to prevent the undesirable interaction of the metal with the semiconductor and to improve significantly the electrical and photoelectric properties of $M-Pb_{1-x}Sn_xTe$ (M = metal) barrier structures.[82]

IV. Electrophysical properties and chemistry of the compound semiconductor–intrinsic oxide interface

In the analysis of the requirements imposed on MOS (or MIS) structures by investigators developing electronic devices, the $Si-SiO_2$ system, which ideally satisfies all these requirements, may serve as a natural reference standard.[1]

The operation of MOS transistors is based on the possibility of inducing in the surface layer of the semiconductor an electric field which regulates the concentration of charge carriers up to the inversion of the type of conduction. The influence of the surface of the semiconductor is especially important in MOS transistors and other devices where the interface is an active region of the device (Schottky barriers, heterojunctions, superlattices). In practice, in order to optimise the parameters of any semiconductor device (dipolar transistor, photodiode, photoresistor), it is neces-sary to protect its surface by an insulator with fully defined characteristics.

Localised surface electronic states (SES),¶ the nature of which may be various, play the main role in all electronic phenomena on the surface and on the interface between the semiconductor and another material. In the first place, these are intrinsic SES arising due to the distortion of the periodic potential of the crystal lattice and the rupture of the chemical bonds involving surface atoms (the Tamm–Shockley levels). In addition, the appearance of SES may be caused by local surface imperfections of the type of structural defects, impurities, and their complexes.

The influence of the SES on the properties of the interface is determined by their charge state, disposition relative to the Fermi level (E_F) and distance from the interface.

A high SES concentration of the order of $10^{14}-10^{15}$ cm^{-2}, which is only a little less than the number of surface atoms, is observed on an atomically clean surface of silicon. The times of the electron exchange between the SES and the bulk phase are very short (less than 10^{-5} s) and such SES are called fast. Their high concentration leads to firm stabilisation of E_F (the so called 'pinning' of the Fermi level) on the surface near the centre of the forbidden gap E_g and it is almost impossible to regulate the properties of the surface with the aid of an external electric field.

During the thermal oxidation of the surface of silicon under optimum conditions, the SES concentration diminishes appreciably (to 10^9 cm^{-2}). This is probably associated with a certain degree of saturation of the ruptured bonds and a weakening of the

¶ The term 'surface electronic states' can be understood literally only for an atomically clean surface. For real interfaces, the SES are distributed in a finite three-dimensional layer.

Tamm factor in the perturbation of the periodic variation of the crystal lattice potential, which diminishes the degree of pinning of the Fermi level and makes it possible to modulate the bending of the bands at the $Si-SiO_2$ interface. However, the presence of structural defects in the oxide leads to the appearance of electron traps (the so called slow SES with a charge transfer time of $10^{-1}-10^{2}$ s).

A characteristic feature of the $Si-SiO_2$ interface is the presence of a built-in charge localised in a narrow (< 2 nm) region, the size and magnitude of which are most important characteristics. In fact it specifies the initial bending of the bands at the silicon surface and hence the conditions in the operation of the MOS transistor (depletion or enrichment). As regards the fast SES, their concentration should be minimal to ensure the maximum efficiency of the regulation of the surface conductivity. As already mentioned, for a high SES density (such as, for example, that at the ACS silicon), this effect is altogether absent. The SES charge transfer times, on which the frequency characteristics of the devices depend, are also important. The number of traps in the oxide should likewise be minimised, since their presence leads to instability of the parameters of the devices as a function of time.

In industrial manufacture, the decisive factor becomes not simply the development of processes ensuring the required parameters of the interface but also their technological suitability and, what is most important, their reproducibility. This requires a deeper understanding of the chemistry of the process in purely empirical developments. The initial advances in the creation of silicon MIS devices, which in the case of binary semiconductors proved useless, are associated with precisely such developments. This is confirmed by the fact that, as early as the 1970s, reports appeared concerning the development of MOS transistors based on GaAs and InP with parameters close to those of the silicon devices but in reality such devices had not been created at the time.

1. Gallium arsenide

Studies of the problem of the segregation of elemental arsenic at the GaAs–oxide interface must be regarded as fundamental. At the beginning of the 1980s, it began to be suspected that it is in fact the presence of As^0 at the interface that makes it unsuitable for the formation of GaAs-based MOS devices.[98] Analysis of the electrical parameters of the GaAs-based MIS structure showed that the concentration of surface electronic states and the position of E_F on the surface are independent of the method of preparation and even of the nature of the insulator (intrinsic oxides grown by means of the electrochemical, anodic, and plasma oxidation, SiO_2, Si_3N_4, $Si_xO_yN_z$, and Al_2O_3), although some dependence of the preliminary treatment of the GaAs surface was noted.[98,99] The density of the surface electronic states, fixing E_F in the vicinity of the middle of E_g, is so high that the bending of the semiconductor bands by the external electric field can be varied within limits insufficient for the attainment of the enrichment conditions or the inversion of surface conductivity.

Studies were carried out on the properties of the ACS of gallium arsenide and the changes in the latter when subjected to controlled influences. It has been established experimentally that there are no surface electronic states in the forbidden gaps of the absolutely clean GaAs and InP surfaces, so that, in contrast to silicon, there is no pinning of E_F on the surface in GaAs and its position is the same as in the bulk phase. However, when extraneous atoms are deposited onto the ACS in amounts appreciably less than a monolayer, the Fermi level in both *n*- and *p*-GaAs shifts approximately to the middle of E_g, where it is fixed and remains unchanged on further increase in the number of adsorbed atoms. Such behaviour of E_F is observed in the adsorption of both different metals and nonmetals, including oxygen.[100]

This made it possible to postulate that the pinning of E_F is caused by the surface electronic states associated with the intrinsic lattice defects and arising on adsorption of extraneous atoms. In the UDM (unified defect model),[101] it was initially assumed that such defects are gallium and arsenic vacancies. However, subsequently calculations and experiments on GaAs bulk phase specimens with different deviations from stoichiometry showed that antistructural defects of the type involving the transfer of arsenic to a Ga sublattice site (As_{Ga}) and conversely the transfer of gallium to an As sublattice site (Ga_{As}) are thermodynamically more favourable in GaAs. In particular, the EL2 trap, which determines many of the characteristic features of GaAs, represents either an isolated As_{Ga} defect or contains an interstitial arsenic atom on the {111} axis.[102] Whereas the appearance of an excess of As in the bulk phase of GaAs is related to the characteristics of its phase diagram,[103] in the oxidation reaction it is related to the GaAs–O structural diagram. Therefore in the approved version of the UDM model — the ADM (advanced defect model)[104] — the main cause of the pinning of E_F is believed to be the antistructural As_{Ga} defect which gives rise to two donor levels. The Fermi level is located between them and the position of E_F depends on the degree of compensation for As_{Ga} by the second defect Ga_{As}, which is an acceptor. An increase in the arsenic content on the surface shifts E_F to the conductivity band, whilst a decrease shifts it in the opposite direction.

One cannot claim that the ADM model fully explains the entire mechanism of the appearance of surface electronic states regulating the position of E_F on the interfaces with GaAs. It may be that effects associated with the presence of impurities, in the given instance adsorbed oxygen [the MIGS (metal induced gap states) model][105] and the disordering of the crystal lattice of the semiconductor in adsorption [the DIGS (defect induced gap states) model],[106] also make a definite contribution.

Convincing evidence that the pinning of E_F is in fact associated with the antistructural defects arising as a consequence of the liberation of arsenic on oxidation has been obtained in a study of thin (~5 nm) epitaxial GaAs layers.[107] The change in the position of E_F can be readily found from the change in the electrical conductivity of such layers on oxidation in air (after their removal from the growth chamber). It has been established that E_F for high-quality epitaxial *n*-GaAs layers, grown at 530 °C, varies nonmonotonically following an increase of exposure in air before becoming fixed. On the other hand, the position of the Fermi level for a similar layer grown at 300 °C does not change at all after exposure to air. Layers obtained at such a low temperature contain up to 5×10^{19} cm^{-3} As_{Ga} defects and their E_F is fixed from the beginning. High-temperature annealing of such layers is known to decrease the concentration of As_{Ga} by more than an order of magnitude. Indeed, the shift of E_F on oxidation for a similar specimen grown at a low temperature but then annealed at 530 °C occurred in the same way as for the usual specimens.

It has been established[108] that the position of E_F for layers grown at low temperatures with an excess of arsenic may be fixed not only by As_{Ga} point defects but also by As^0 precipitates segregated in the bulk of the material.† The position of E_F changes by more than 0.2 eV on passing from one pinning mechanism to another.

The changes in the electrophysical parameters of the GaAs-based MOS transistors may be caused not only by their thermodynamic instability, due to reaction (1), but also by the precipitation of As^0 on the interface described above.

The relation between the presence of As^0 and As_2O_3 on the GaAs surface and the fixation of the Fermi level has been confirmed by experiments involving the washing of the GaAs surface with water.[111] As_2O_3 is soluble in water, whereas As^0 dissolves in water only if the specimen has been illuminated with fairly intense light inducing photochemical reactions or if the water has been saturated with oxygen. In this case, As^0 is initially oxidised to As^{3+}, which then dissolves in water. Experiment shows that the intensity of the photoluminescence, which depends on the degree of fixation of E_F, increases appreciably only when

† The so called internal Schottky barrier model,[109] which permits a new approach to the problem of semi-insulating semiconductors.[110]

the GaAs specimens have been washed in a stream of water saturated with O_2 or under illumination. This leads to the washing away of both As_2O_3 and As^0. However, after storage for several minutes in air, especially at an elevated temperature, the photoluminescence intensity falls to the previous level, which is associated with the reoxidation of the GaAs surface. The new stage involving washing with water again increases the brightness of the luminescence and this cycle can be repeated several times.

Treatment of the GaAs surface with a $Na_2S.9H_2O$ solution also leads to an appreciable increase in the effectiveness of the photoluminescence.[112,113] A series of methods have been developed for the treatment of the GaAs surface with sulfides, which greatly diminishes the rate of surface recombination. After such treatment, the oxides are removed from the GaAs surface and an ideal crystal lattice is created on the latter, in the first layer of which the sulfur atoms substitute all the arsenic atoms and form thermodynamically stable bonds with gallium atoms (Fig. 8).

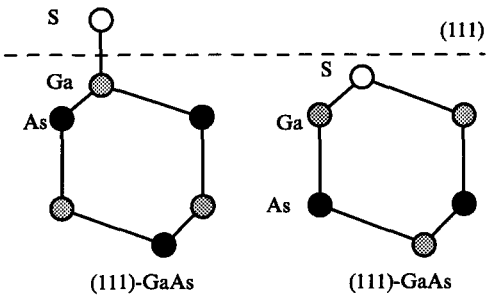


Figure 8. Distribution of sulfur atoms on the (111) surface of GaAs passivated with sulfur.[2,149]

The importance of the complete removal of arsenic is indicated by the comparison of the efficiencies of the treatment of the GaAs surface with Na_2S and $(NH_4)_2S$ solutions.[114] Experiments with a layer of arsenic especially sputtered on showed that, in contrast to Na_2S, the $(NH_4)_2S$ solution effectively dissolves arsenic. Sulfidation with this solution actually leads to a more than twofold decrease in the density of surface traps and hence to a decrease in the rate of surface recombination. However, since the heats of formation of sulfides are lower than those of the corresponding oxides, a GaAs surface treated with sulfide solutions is unstable on storage in air and in the course of several days the initial properties of the surface are restored.

All the experiments involving the study of the stability of the GaAs surface freed from As by different methods have shown that the reason for the subsequent appearance of arsenic is reoxidation. Therefore all the technological processes for the creation of an insulator–GaAs interface must be devised in such a way that the oxidation of the GaAs surface is ruled out.

In the plasmochemical etching methods, it is technologically easy to combine in a single cycle the cleaning of the GaAs surface and the deposition of insulators. An example is provided by the etching of the surface in a hydrogen HF plasma with subsequent deposition of Ga_2O_3,[115] which is thermodynamically stable in relation to GaAs. The protecting layer is generated by evaporating gallium in an oxygen plasma. In order to rule out the reoxidation of GaAs under these conditions, the GaAs specimens are additionally etched in a nitrogen plasma, which creates a thin layer of arsenic nitride saturating the free arsenic bonds. The interfaces thus obtained have a low density of surface electronic states and the E_F level is not fixed. Under these conditions, degradation of the parameters was not observed even after storage of the specimens for several months in air.

It has been established[116] that treatment of the GaAs surface in a CF_4 plasma before depositing Si_3N_4 leads to the effective removal of As^0 and As_2O_3 and also to the formation of a passivating layer made up of Ga_2O_3 and GaF_3. Such a passivating coating greatly improves the characteristics of high-power GaAs-based transistors and prolongs their working life. The stability of the interface can be achieved also by the direct deposition of GaF_3 if the GaAs surface has been subjected to a preliminary treatment in $(NH_4)_2S$ solution.[117]

Another method for producing an ideal interface involves not the removal of the oxides from the GaAs surface but their reduction. This can be carried out by depositing a thin layer of silicon on the GaAs surface. For a correctly selected thickness of the layer (~0.8 nm) and of the temperature of the subsequent annealing, it is possible to reduce the oxides on GaAs completely and a layer of SiO_2 with a specified thickness can be deposited on the structure thus obtained.[118]

It is noteworthy that the understanding of the chemistry of all processes leading to the oxidation of the GaAs surface has actually made it possible in recent years to take definite steps towards the creation of GaAs-based MIS devices.

2. Indium phosphide

It follows from the phase equilibrium diagram that the chemistry of the InP–intrinsic oxide interface is qualitatively different. It is of interest to elucidate how this is reflected in the electrophysical properties of MOS structures.

When oxygen is adsorbed, E_F on the InP surface is also fixed but not in the middle of E_g, as in GaAs, but closer to the bottom of the conductivity band (as a result of an intrinsic lattice defect different from that in GaAs).[101] In combination with the fact that the density of surface electronic states on the interface involving InP is an order of magnitude lower than in GaAs, this makes it possible to achieve different versions of InP-based MOS transistors.[99] Slow surface electronic states and traps, which lead to a prolonged drift of the characteristics, are always present on the interfaces obtained between InP and intrinsic oxides as well as other insulators.

The effects associated with the instability of the characteristics can be eliminated by employing thin (< 30 nm) oxide layers[119] consisting only of the phosphate $In(PO_3)_3$, in which the width of the forbidden gap is fairly considerable ($E_g \simeq 7$ eV). Under these conditions, the edge of the conduction band E_c in the oxide is higher by 2.3 eV than in InP, which ensures an adequate potential barrier preventing the injection of electrons from InP into the oxide.[56] In the case of thick oxide films, the outer layer of which consists partly of In_2O_3 having an appreciably lower E_g (~ 3.5 eV), the difference $E_c(In_2O_3) - E_c(InP)$ is apparently also small. This leads to the possibility of the tunnelling of electrons from InP through $In(PO_3)_3$ and into In_2O_3.[120] This factor is apparently the cause of the marked frequency dispersion and the hysteresis characteristics of the MOS capacitors prepared on the basis of thick oxides. Having etched away the outer layer of the anodic oxide leaving only the layer consisting of $In(PO_3)_3$, it is possible to eliminate the deficiencies noted above. Furthermore, this operation greatly diminishes the hygroscopicity of the specimens. Thus, whereas after the storage of unetched specimens for several hours in air an appreciable increase in the thickness of the initial anodic oxide (up to 40%) is observed, for the anodic oxide with an etched outer layer such a change is much slower (up to 30% in one month). Furthermore, annealing of an anodic oxide of this kind at 250 °C in nitrogen for 30 min stabilises its properties. Having sputtered a layer of Al_2O_3 onto it with a thickness of 100 nm, it was possible to obtain, on the basis of a semi-insulating InP substrate, a transistor with significantly more stable characteristics.[56]

Having selected the plasma oxidation conditions in such a way that the contents of In_2O_3 and P_2O_5 are reduced to a minimum, it is possible to obtain an interface with nearly theoretical electrical parameters.[61]

Under optimal conditions, the interface between InP and an intrinsic oxide is sufficiently ideal. During its formation, it is important to eliminate (bearing in mind the low thermal and

radiation stabilities of the InP surface) the possibility of both a general structural disordering[106,121] and of the appearance of intrinsic lattice defects. For example, the phosphorus vacancies arising during the annealing of an absolutely clean (100) surface of InP in vacuo lead to an appreciable alteration of its properties and, in the view of a number of investigators, are responsible for the pinning of E_F.[122] One cannot also exclude the possibile formation on the InP surface of other types of intrinsic defects which may exist in the bulk of InP in the presence of an excess of one of the components.[123–125] This has been clearly demonstrated by Hu et al.,[127] who obtained the oxide by plasma oxidation under the conditions which excite electron cyclotron resonance. This process is closer to thermal than to anodic oxidation, although it does occur at room temperature. Indeed, after the formation in the plasma of an oxide film 9 nm thick, an appreciable amount of elemental phosphorus appears at the InP–intrinsic oxide interface according to XPES data. It was possible to eliminate this effect by placing a screen between the source of plasma and the InP surface, which greatly reduced the rate of growth of the oxide film (by a factor greater than 2) but eliminated the direct bombardment of the InP surface by high-energy ions. A layer of SiO_2 having a thickness of 70 nm was grown by the same method on the oxide 3 nm thick obtained in this way. The structures with the oxide grown in shielded plasma have a very low density of fast and slow surface electronic states.

3. Semiconductor solid solutions

Fairly satisfactory properties of the interface were obtained already in the first experiments on the formation of CdTe-based MOS structures. The phase equilibrium diagram for this compound also predicts equilibrium oxidation with formation of only one compound (Fig. 1*b*). Anodic,[128] thermal, chemical, and plasma[129] oxidation reactions were tested, but the best parameters of the interface and of the insulator itself were obtained for the thermal oxide. The properties of the MOS structures depend in many respects on the initial treatment of the semiconductor surface. It is not fortuitous that the best parameters were obtained after the preliminary annealing of CdTe under an atmosphere of hydrogen, which restores the stoichiometry of the CdTe surface disturbed by chemical polishing.

Despite the complexity of the chemical reactions occurring in the oxidation of $Hg_{1-x}Cd_xTe$, only $CdTeO_3$ is present at its interface with the anodic oxide (Fig. 6*a*). This is precisely why the interface before annealing has a very low density of the fast and slow surface electronic states, which is actually comparable to the density at the $Si-SiO_2$ interface.[24,72] It has been shown[24] that the (100) surface of $Hg_{1-x}Cd_xTe$ can be brought into virtually ideal conformity with the (011) surface of $CdTeO_3$, which has the perovskite crystal lattice. This minimises the number of ruptured bonds at the interface. The interfaces between $Hg_{1-x}Cd_xTe$ and the anodic sulfide[88] and fluoride[89] also have a low density of the fast and slow surface electronic states. In the former case, this is associated with the fact that the interface actually represents a heterojunction formed by II–VI solid solutions, while the reason for the latter is that the cadmium oxide fluoride (Fig. 7*b*), the parameters of which are close to those of $CdTeO_3$, is always actually present at the $Hg_{1-x}Cd_xTe$–fluoride interface.

A high built-in charge, which always has a positive sign, is characteristic of the $Hg_{1-x}Cd_xTe$–anodic oxide interface. It has been suggested that the positive sign is due to positively charged oxygen vacancies.[72] This agrees well with the mechanism of ion transport during the growth of the anodic oxide and also with data for the cathodoluminescence of the anodic oxide on $Hg_{1-x}Cd_xTe$.[130] The latter data show that the radiative recombination centres are associated with the deficiency of oxygen in TeO_2 or in more complex compounds based on it. A significant disadvantage of the anodic oxide on $Hg_{1-x}Cd_xTe$ is its low thermal stability. Heating of *n*-type specimens at relatively low temperatures leads to an increase in the built-in charge, while heating of the *p*-type specimens results in the inversion of the type of conductivity, the thickness of the *n*-type layer produced reaching 40 μm depending on the temperature and duration of the annealing.[74–76] The mercury accumulated at the interface during anodic oxidation diffuses during annealing to the bulk of the crystal and is annihilated on recombining with mercury vacancies. This accounts for the inversion of the type of conductivity. The reactions occurring at the interface during annealing may serve as an additional source of mercury.

The $Hg_{1-x}Cd_xTe$ surface acquires *n*-type conductivity during natural, anodic, and plasma oxidations. On the other hand, the conductivity of the surfaces of PbSe, $Pb_{1-x}Sn_xSe$,[131] and $Pb_{1-x}Sn_xTe$ [132] is always of the *p*-type. Comparison of the phase equilibrium diagrams for $Hg_{1-x}Cd_xTe$ and lead and tin chalcogenides suggested[133] that the preferential oxidation of the chalcogen in the former case and of the metal in the latter is in fact responsible for the opposite type of surface conductivity in these materials. The presence of free chalcogen or metal atoms at the interface, appearing as a consequence of such oxidation, can exert a decisive influence on the entire assembly of defects in the oxide responsible for the built-in charge. This is indicated by data on the cathodoluminescence of the anodic oxides on $Hg_{1-x}Cd_xTe$ [130] and $Pb_{1-x}Sn_xTe$,[134] demonstrating the different nature of the radiative recombination centres. Furthermore, differences are manifested also in the mechanisms of mass transfer during the growth of anodic oxides on the surfaces of both materials.[69,135] As a consequence of the excess of one of the components on the interface, as in the case of As in GaAs, the concentration of the intrinsic lattice defects increases. Different point defects, whose electrical behaviour and influence on the diffusion processes in the semiconductor have not yet been finally established, may occur in mercury and lead chalcogenides.[136–138] However, one may expect that their contributions to the properties of the interface will be different.

The same phenomena have been observed in the study of the $Hg_{1-x}Zn_xTe$–anodic oxide interface, where both the metal and the chalcogen are liberated according to the phase equilibrium diagram (Fig. 3*b*). The differences between the properties of the $Hg_{1-x}Zn_xTe$–anodic oxide and $Hg_{1-x}Cd_xTe$–anodic oxide interfaces can be accounted for by the competing influence of the elemental tellurium appearing in the region of the interface.[133] Firstly, the magnitude of the built-in charge in the $Hg_{1-x}Zn_xTe$-based MOS structures is smaller than in the analogous $Hg_{1-x}Cd_xTe$-based structures.[139–141] Secondly, the layer with *n*-type conductivity on $Hg_{1-x}Zn_xTe$ arises at higher annealing temperatures and its thickness is smaller by a factor of 2 than that of the anodic oxide on $Hg_{1-x}Cd_xTe$ obtained under similar conditions. This indicates a small amount of mercury liberated at the $Hg_{1-x}Zn_xTe$–anodic oxide interface. Similar changes are also observed during annealing for the $Hg_{1-x}Mn_xTe$–anodic oxide system.[75,142] Since the zinc and manganese contents in the solid solutions investigated are low compared with the mercury contents, the liberation of tellurium is insignificant compared with mercury and there is a correspondingly small compensating effect.

The changes in the properties of the $Hg_{1-x}Cd_xTe$–anodic sulfide (or fluoride) interface are greater than the changes in the properties of the $Hg_{1-x}Cd_xTe$–anodic oxide interface. According to the phase equilibrium diagrams, mercury should not be liberated at all at the interface in such systems. Indeed, the sign of the built-in charge for the anodic sulfide is reversed,[88] while that for the fluoride, although remaining positive, is an order of magnitude smaller compared with the anodic oxide and its magnitude is to a large extent regulated by the conditions in the electrochemical process.[89] Finally, on heating both the sulfide and fluoride on $Hg_{1-x}Cd_xTe$, an *n*-type layer does not arise,[75,142] which indicates the absence of the liberation of mercury at the $Hg_{1-x}Cd_xTe$–intrinsic insulator interface.

V. Current trends in the development of insulators for metal – insulator – semiconductor devices and protection of the surfaces of compound semiconductors

1. Gallium arsenide

In the development of a technology for the formation of GaAs-based insulators, it was necessary to exclude the possibility of the fortuitous oxidation of the semiconductor surface, for example on contact with the atmosphere between individual operations, and of a side oxidation reaction as a consequence of some kind of secondary process. New intrinsic defects of the As_{Ga} antistructural defect type must not arise under these conditions and structural disordering of the interface must not occur, i.e. it is essential to exclude all factors inducing the appearance of surface electronic states.

A theoretically ideal semiconductor–insulator interface can be obtained by growing epitaxial layers of a single crystal insulator on the semiconductor. Such insulators may be the alkaline earth metal fluorides CaF_2 and SrF_2. On evaporation in an ultrahigh vacuum, these materials sublime without dissociating, which makes it possible to obtain stoichiometric single crystal layers with the aid of molecular beam epitaxy. MIS structures based on the GaAs–SrF_2 and GaAs–CaF_2 systems have been investigated.[144,145] The differences between the types of chemical bonds as well as the lattice constants and thermal expansion coefficients of these fluorides and III–V semiconductors are responsible for the high density of surface electronic states at the interface, although it can in fact be diminished by rapid annealing. Best results have been obtained with the aid of the epitaxy of cubic gallium sulfide.[146,147] Bearing in mind that the discrepancy between the lattice constants of the two compounds is small and that the sulfur in gallium sulfide is satisfactorily compatible with the GaAs lattice (Fig. 8), it is possible to obtain an ideal interface with parameters indicating that there are good prospects for the practical employment of such structures.

An ideal interface can also be obtained by employing semiconductors of the same III–V group in which the width of the forbidden gap is large (quasi-insulators). The lattice constants of these semiconductors and GaAs should agree. A satisfactory interface with a low density of surface electronic states and a high stability has been obtained for the GaAs–$Al_xGa_{1-x}As$ structure,[148] but the gap between the bands of the insulator and the semiconductor is then too narrow (only 0.4 eV) to prevent the transfer of electrons from the semiconductor to the insulator. A larger gap between the bands exists in another couple, namely GaAs–ZnSe.[2]

Two-layer structures, in which the first layer, without adequate chemical stability primarily towards atmospheric oxygen, forms an interface with the required electrical parameters, while the second performs protecting functions, are promising.[2] According to the authors,[2] interfaces with GaAs having nearly ideal parameters are ensured by a monolayer of antimony, which gives rise to an ordered structure of the (110) surface of GaAs in which there are no ruptured bonds. The principal problem under these conditions is the creation of a second layer: it must be formed without disturbing the properties of the GaAs–Sb interface. This is achieved by sputtering on CaF_2. At any rate the GaAs surface passivated by sulfur remains stable after the deposition of CaF_2 even on annealing at temperatures up to 410 °C.[149]

Amorphous or crystalline germanium or silicon layers can also be employed as an intervening layer. The GaAs–Si–SiO_2, GaAs–Si–Si_3N_4, and GaAs–Si–AlN structures have been vigorously investigated recently.[150] The best results were obtained for GaAs–Si–Si_3N_4 when a layer of silicon was grown in the presence of atomic hydrogen. The parameters of such MIS structures approach those of the Si–SiO_2 system. This permits the hope that, by employing precisely this technology, it will be finally possible to create GaAs-based MIS devices.

2. Indium phosphide

The parameters of the InP–oxide interface are significantly higher than those of the GaAs–oxide interface. It is believed[150] that further improvement of the characteristics may be achieved only by employing a technology which excludes any kind of oxidation. Therefore many of the methods described above are used also for InP. These include epitaxy of the alkaline earth metal fluorides CaF_2[151] and $Ba_{1-x}Sr_xF_2$[152] and of the quasi-insulators $In_xAl_{1-x}As$.[144] Interesting results have been obtained for InP (as for GaAs) on deposition of an antimony monolayer.[122] However, it is still too early to speak of InP-based devices.

More promising results have been obtained on deposition of phosphorus[153] or boron[154] nitrides. However, it is then necessary to carry out the process under mild conditions which rule out a disturbance of the stoichiometry of the InP surface.

At the same time, the form of the phase equilibrium diagram for the InP–O system suggests that, in order to improve the parameters of InP-based MIS devices, there is no need at all to avoid oxidation but it is necessary to optimise the process in such a way that a thermodynamically stable phosphate phase is grown on the InP surface. This view is supported by the continuing development of different methods for the creation of oxide films — by anodic,[56] plasma,[61,155] photochemical,[156] and thermal[51] oxidation and by the thermal evaporation of P_2O_5.[157]

3. Semiconductor solid solutions

Intrinsic insulators are used quite widely for the passivation of the surfaces of devices based on $Hg_{1-x}Cd_xTe$ as a layer forming an interface with the semiconductor. The anodic oxide combined with thermally sputtered ZnS is used in photoresistors,[158,159] whilst the anodic sulfide in the same combination is employed in photodiodes.[6,160] Their main disadvantage is their low thermal stability. Some improvement is afforded by the replacement of the anodic oxide by the anodic fluoride.[6]

It is believed that a radical improvement of the properties of the $Hg_{1-x}Cd_xTe$–intrinsic insulator interface and of the thermal stability will be achieved by employing as the quasi-insulator wide-band semiconductors of the same group — CdTe and $Cd_{1-x}Zn_xTe$[159–162] and of $Cd_{1-x}Mn_xTe$ for $Hg_{1-x}Mn_xTe$.[163] These materials have a much higher E_g compared with the protected semiconductor, which makes the use of quasi-insulators in this case much more effective than for III–V semiconductors. The satisfactory correspondence of the crystal lattices makes it possible to obtain, using different epitaxial methods, an almost ideal interface between such semiconductors and $Hg_{1-x}Cd_xTe$.

The electrochemical methods for the generation of CdTe[164,165] on the $Hg_{1-x}Cd_xTe$ surface are also of interest. A single crystal interface cannot be obtained with their aid owing to the low process temperature, but it is possible to combine in one technological operation the precision chemical cleaning of the $Hg_{1-x}Cd_xTe$ surface and the deposition of CdTe. Interesting results have been obtained on electrochemical reconstruction of the $Hg_{1-x}Cd_xTe$ surface layer on ZnTe on which a layer of ZnS was subsequently deposited by means of gas-phase epitaxy.[166]

In conclusion one should note that the possibilities of generating on $Hg_{1-x}Cd_xTe$ a high-quality interface with the aid of classical insulators such as Al_2O_3,[167] SiO_2,[168] and their combinations[169] cannot be regarded as fully exhausted. Thus the best parameters of the interface for the $Hg_{1-x}Zn_xTe$ solid solution have in fact been obtained with the aid of SiO_2.[140] Incidentally, despite the disadvantages mentioned above, even oxidation has found an application in the creation of lasers based on $Al_xGa_{1-x}As$–GaAs quantum-well heterostructures[170,171] by virtue of the excellent optical characteristics of the oxides.

* * *

Comparison of the entire set of experimental data obtained in studies of compound semiconductor–intrinsic insulator interfaces with the corresponding phase equilibrium diagrams has shown that in many instances there is a direct relation between the characteristics of the phase diagrams such as segregation of the metal or the nonmetal and the intrinsic lattice defects arising under these conditions, on the one hand, and the electrophysical parameters of the interface, on the other.

All this demonstrates that the ideas underlying the models of intrinsic defects[101,104] for the III–V compounds are fully applicable also to the analysis of the interfaces involving the II–VI and IV–VI semiconductors.

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